

IN THE CLAIMS:

All claims have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A DRAM circuit comprising:

a substrate ~~having a~~ ~~an~~ having an active region thereon and ~~a~~ capacitor structure disposed above ~~said~~ the active region, ~~the~~ said capacitor structure including a storage node, a dielectric layer overlying ~~the~~ said storage node, and a conductive cell plate overlying ~~the~~ said dielectric layer, each of ~~the~~ said dielectric layer and ~~the~~ said conductive cell plate having an end portion proximate a conductive contact, ~~the~~ said conductive contact extending

downward and adjacently beside ~~the~~ said capacitor structure, ~~the~~ said end portion of ~~the~~ said dielectric layer extending closer to ~~the~~ said conductive contact than ~~the~~ said end portion of ~~the~~ said conductive cell plate;

a first TEOS layer disposed proximate ~~the~~ said storage node;

a second TEOS layer disposed over ~~the~~ said capacitor structure and encasing ~~said~~ the end portions of ~~the~~ said dielectric layer and ~~the~~ said conductive cell plate, ~~said~~ the second TEOS layer disposed between ~~said~~ the capacitor structure and ~~said~~ the conductive contact; and

a doped BPSG layer disposed over ~~said~~ the second TEOS layer, ~~said~~ the conductive contact extending through ~~said~~ the BPSG layer and ~~said~~ the second TEOS layer.

Claims 2-3 (Canceled)

4. (Currently Amended) The DRAM circuit of claim 1, wherein each of ~~said~~ the storage node and ~~the~~ said conductive cell plate are heavily doped with dopants.

5. (Currently Amended) The DRAM circuit of claim 1, wherein each of said-the storage node and the said-conductive cell plate comprise a phosphorous-doped polysilicon.
6. (Currently Amended) The DRAM circuit of claim 1, wherein the said-dielectric layer comprises a capacitor cell dielectric layer.
7. (Currently Amended) The DRAM circuit of claim 1, wherein said-the dielectric layer comprises a nitride layer.
8. (Currently Amended) The DRAM circuit of claim 1, wherein said-the capacitor structure comprises a container-shaped capacitor.
9. (Currently Amended) The DRAM circuit of claim 1, wherein the said-second TEOS layer is a dopant barrier between the said-capacitor structure and said BPSG layer.
10. (Currently Amended) A semiconductor memory device comprising:
a semiconductor substrate having an active region thereon and a capacitor structure formed above the said-active region, said-the capacitor structure including a first conductive layer, a second conductive layer, and a dielectric layer, the said-dielectric layer disposed between said-the first and second conductive layers, each of said-the dielectric layer and the said-first and second conductive layers having an end portion proximate a conductive contact, said-the conductive contact extending downward and adjacently beside said-the capacitor structure, said-the end portion of said-the dielectric layer extending closer to said-the conductive contact than said-the end portion of each of the said-first conductive layer and said-the second conductive layer;
a diffusion barrier proximate the said-first conducting layer and configured to prevent diffusion of contaminants into said-the active region;

a TEOS layer disposed over said-the capacitor structure and encasing said-the end portions of the said dielectric layer and each of said-the first conductive layer and said-the second conductive layer, said-the TEOS layer disposed between said-the capacitor structure and said-the conductive contact; and
a doped BPSG layer disposed over said-the TEOS layer, the said-conductive contact extending through said-the BPSG layer and said-the TEOS layer.

Claims 11-12 (Canceled)

13. (Currently Amended) The device of claim 10, wherein said-the conductive contact comprises at least one of metal and conductively doped polysilicon.

14. (Currently Amended) The device of claim 10, wherein said-the conductive contact comprises a digit line.

15. (Currently Amended) The device of claim 10, wherein each of said-the first conductive layer and said-the second conductive layer are heavily doped with dopants.

16. (Currently Amended) The device of claim 10, wherein each of the said-first conductive layer and said-the second conductive layer comprise a phosphorous-doped polysilicon.

17. (Currently Amended) The device of claim 10, wherein said-the dielectric layer comprises a capacitor cell dielectric layer.

18. (Currently Amended) The device of claim 10, wherein said-the dielectric layer comprises a nitride layer.

19. (Currently Amended) The device of claim 10, wherein the said-capacitor structure comprises a container-shaped capacitor.

20. (Currently Amended) The device of claim 10, wherein said-the TEOS layer is a dopant barrier between the said-capacitor structure and said-the BPSG layer.

21. (Currently Amended) The DRAM circuit of claim 1, wherein said-the first TEOS layer is configured to prevent diffusion of contaminants into said-the active regions.

22. (Currently Amended) The DRAM circuit of claim 1, wherein said-the first TEOS layer comprises a thickness of about 100 Å to about 250 Å.

23. (Currently Amended) The semiconductor memory device of claim 10, wherein said the diffusion barrier comprises a nitride layer or TEOS layer.

24. (Currently Amended) The semiconductor memory device of claim 10, wherein said the diffusion barrier comprises a thickness of about 100 Å to about 250 Å.